REMARKS/ARGUMENTS

The Office Action mailed June 5, 2003, has been received and reviewed. Claims 1 through 62 are currently pending in the application. Claims 2, 9, 17 through 23, 25, 32, and 40 through 62 are withdrawn from consideration as being drawn to non-election inventions. Claims 1, 3 through 8, 10 through 16, 24, 26 through 31, and 33 through 39 stand rejected.

Per this response, Applicant has cancelled claims 47 through 62, amended claims 1, 6, 8, 9, 12-14, 18, 22-24, 29, 31, 32, 35, 37, 41, 45 and 46, and respectfully requests reconsideration of the application as amended herein.

Information Disclosure Statement(s)

Applicant notes the filing of an Information Disclosure Statement herein on June 2, 2003, and notes that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 be made of record herein.

Drawings

The Examiner states that the proposed drawing correction and/or the proposed substitute sheets of drawings, filed on October 29, 2002, have been approved. The Examiner further states that a proper drawing correction or corrected drawings are required in reply to the Office Action in order to avoid abandonment and that such correction to the drawings will not be held abeyance. Applicant notes that the drawings filed on October 29, 2002, included corrected formal drawings. Nevertheless, Applicant resubmits, herewith, formal drawings which incorporate the previously submitted drawing corrections.

35 U.S.C. § 112 Claim Rejections

Claim 13 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. More particularly, the Examiner states that the limitation "the at least two apertures"

in line 3 of claim 13 lacks proper antecedent basis. Applicant has amended claim 13 herein to remove any perceived ambiguity and provide proper antecedent basis.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,228,862 to Baumberger et al.

Claims 1, 3 through 8, 10, 12 through 14, 24, 26 through 31, and 35 through 37 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Baumberger et al. (U.S. Patent No. 5,228,862). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1, 3 through 8 and 12 through 14

Independent claim 1, as amended herein, is directed to a method of aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween. The method comprises: *forming at least two channels through the semiconductor device package from a first major surface thereof to a second, opposing major surface thereof*; providing a major surface of the carrier substrate with at least two alignment features spaced and positioned in respective correspondence to the at least two channels; placing the semiconductor device package over the carrier substrate; and *aligning the at least two channels formed in the semiconductor device package with the at least two alignment features of the carrier substrate.* Applicant respectfully submits that Baumberger fails to teach all of the limitations of claim 1 of the presently claimed invention.

The Examiner cites Baumberger as teaching "a method of aligning comprising: forming at least two channels (41) through a semiconductor device (10); providing a major surface of a carrier substrate (11, 13) with at least two alignment features (41); placing the semiconductor device over

the carrier substrate and aligning the at least two channel[s] with the at least two alignment features (see Figs. 1-3)." (Office Action, page 3). Applicant respectfully disagrees.

Baumberger is directed to a fluid actuated connector for interconnecting opposed circuit members such as circuit modules or printed circuit boards. Baumberger states that "the term circuit module is meant to include a substrate or the like member having various electrical components (e.g., semiconductor chips, conductive circuitry, conductive pins, etc.) which may form part thereof." (Col. 2, line 68 – col. 3 line 4). Additionally, the circuit module (11) described by Baumberger "may ... include *semiconductor devices (chips) 18* on [a] surface and coupled to designate elements 19." (Col. 3, lines 30-33, emphasis added).

Baumberger further states that "the term printed circuit board is meant to define a substrate including therein at least one (and, typically, several) conductive layer which in turn may provide signal, power and/or ground functions." (Col. 3, lines 8-11).

The connector (10), which the Examiner identifies as a semiconductor device, includes an upper and a lower surface (24, 24) which are sealingly coupled to one another by flexible members (27, 29). A plurality of conductors (33) are disposed on each of the upper and lower surfaces for selective interconnection with corresponding conductive elements (19) on either the circuit module (11) or the circuit board (13). Flexible circuitized elements (35) provide interconnection between the conductive elements on the upper surface and the lower surface of the connector. The connector is generally disposed between the circuit module and the circuit board in a spaced relationship therewith. When a fluid pressure is provided to the sealed, internal portion of the connector, the upper and lower surfaces are displaced away from each other to establish physical and electrical contact with the conductive elements of the circuit module and the circuit board respectively. (See, e.g., col. 4, line 13 – col. 5, line 50; FIGS. 2 and 3).

A pair of elongated pins 41 pass through apertures formed in each of the connector, the circuit module and the circuit board, to effect alignment thereof. However, Applicant notes that the elongated pins of Baumberger do not pass through any of the semiconductor devices (18) disposed on the circuit module. Nor does Baumberger teach any method of aligning the

semiconductor devices with the circuit module. As such, Applicant submits that claim 1 is clearly not anticipated by Baumberger.

Applicant further submits that claims 3 through 8 and 12 through 14 are also allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 4, Applicant submits that Baumberger fails to teach forming at least two blind holes in a carrier substrate as alignment features associated therewith.

With respect to claim 6, Applicant submits that Baumberger fails to teach forming the pins of an electrically nonconductive material. While Baumberger states that "other" materials may be used, the preferred embodiment includes stainless steel pins indicating that electrically conductive pins are desirable. There does not appear to be any teaching by Baumberger to the contrary.

With respect to claim 7, Applicant submits that Baumberger fails to teach forming the pins of an anti-static material.

With respect to claim 8, Applicant submits that Baumberger fails to teach affixing the pins to a *semiconductor device package*.

With respect to claim 12 through 14, Applicant submits that Baumberger fails to teach placing a semiconductor device package over a carrier substrate using a pick and place device.

With respect to claims 13 and 14, Applicant submits that Baumberger fails to teach inserting pins carried by the head of the pick and place device through the at least two channels and the at least two holes.

With respect to claim 14, Applicant submits that Baumberger fails to teach lifting the pick and place device, including the pins, from the aligned semiconductor device package and carrier substrate.

Applicants, therefore, respectfully request reconsideration and allowance of claims 1, 3 through 8 and 12 through 14.

Claims 24, 26 through 31 and 35 through 37

Independent claim 24, as amended herein, is directed to a method of testing a semiconductor device package having a plurality of discrete conductive elements disposed in a pattern on a surface thereof. The method comprises: providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements; *forming at least two channels in the semiconductor device package, each channel passing from a first surface thereof to a second, opposing surface thereof*; providing the carrier substrate with at least two alignment features, each alignment feature respectively spaced and positioned in correspondence to one of the at least two channels; placing the semiconductor device package over the carrier substrate; a*ligning each channel of the at least two channels formed in the semiconductor device package with a corresponding alignment feature of the at least two alignment features of the carrier substrate*; electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality; and passing at least one electrical signal between the semiconductor device package and the carrier substrate. Applicant respectfully submits that Baumberger fails to teach all of the limitations of claim 24 of the presently claimed invention.

Again, the Examiner cites Baumberger as teaching "a method of aligning comprising: forming at least two channels (41) through a semiconductor device (10); providing a major surface of a carrier substrate (11, 13) with at least two alignment features (41); placing the semiconductor device over the carrier substrate and aligning the at least two channel[s] with the at least two alignment features (see Figs. 1-3)." (Office Action, page 3). Applicant respectfully disagrees.

As set forth above, Baumberger is directed to a fluid actuated connector for interconnecting opposed circuit members such as circuit modules or printed circuit boards (as defined therein). The connector (10), which the Examiner identifies as a semiconductor device, is configured to provide electrical contact with the circuit module (11) and the circuit board (13) upon actuation thereof by a pressurized fluid. (See, e.g., col. 4, line 13 – col. 5, line 50; FIGS. 2 and 3). A pair of elongated pins 41 pass through apertures formed in each of the connector, the circuit module and the circuit board, to effect alignment thereof.

However, Applicant notes that the elongated pins of Baumberger do not pass through any of the semiconductor devices (18) disposed on the circuit module. Nor does Baumberger teach any method of aligning the semiconductor devices with the circuit module. As such, Applicant submits that claim 24 is clearly not anticipated by Baumberger.

Applicant further submits that 26 through 31 and 35 through 37 also allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter set forth thereby.

With respect to claim 26, Applicant submits that Baumberger fails to teach forming at least two blind holes in a carrier substrate as alignment features associated therewith.

With respect to claim 29, Applicant submits that Baumberger fails to teach forming the pins of an electrically nonconductive material. While Baumberger states that "other" materials may be used, the preferred embodiment includes stainless steel pins indicating that electrically conductive pins are desirable. There does not appear to be any teaching by Baumberger to the contrary.

With respect to claim 30, Applicant submits that Baumberger fails to teach forming the pins of an anti-static material.

With respect to claim 31, Applicant submits that Baumberger fails to teach affixing the pins to a *semiconductor device package*.

With respect to claim 35 through 37, Applicant submits that Baumberger fails to teach placing a semiconductor device package over a carrier substrate using a pick and place device.

With respect to claims 36 and 37, Applicant submits that Baumberger fails to teach inserting pins carried by the head of the pick and place device through the at least two channels and the at least two holes.

With respect to claim 37, Applicant submits that Baumberger fails to teach lifting the pick and place device, including the pins, from the aligned semiconductor device package and carrier substrate.

Applicants, therefore, respectfully request reconsideration and allowance of claims 24, 26 through 31 and 35 through 37.

Anticipation Rejection Based on U.S. Patent No. 3,678,385 to Bruner

Claims 1, 12 through 16, 24, and 35 through 39 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bruner (U.S. Patent No. 3,678,385). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claims 1 and 12 through 16

Independent claim 1, as amended herein, is directed to a method of aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween. The method comprises: *forming at least two channels through the semiconductor device package from a first major surface thereof to a second, opposing major surface thereof*; providing a major surface of the carrier substrate with at least two alignment features spaced and positioned in respective correspondence to the at least two channels; placing the semiconductor device package over the carrier substrate; and *aligning the at least two channels formed in the semiconductor device package with the at least two alignment features of the carrier substrate*. Applicant respectfully submits that Bruner fails to teach all of the limitations of claim 1 of the presently claimed invention.

The Examiner cites Bruner as teaching "a method of aligning comprising: forming at least two channels (28) through a semiconductor device (2); providing a major surface of a carrier substrate (3) with at least two alignment features (12); placing the semiconductor device over the carrier substrate and aligning the at least two channel[s] with the at least two alignment features (see Figs. 1 and 5)." (Office Action, page 3). Applicant respectfully disagrees.

Bruner discloses a device for assembling and testing microelectronic circuit members. The device includes a lead frame holder (2), which the Examiner identifies as a semiconductor device, and a cap (3), which the Examiner identifies as a carrier substrate. The lead frame holder includes a plurality of aligned channels, each being configured to receive a lead (17) of a lead frame. The lead frame holder also includes an opening configured to receive a substrate (19) therein such that the leads of the lead frame are aligned with conductive terminals of the substrate. The cap then

engages the lead frame holder and applies pressure to the lead frame such that individual leads are pressed against associated substrate terminals. (See, e.g., col. 1, line 70 – col. 2, line 20; FIG. 1). Bifurcated latching members (12) are configured to engage holes (28) of the lead frame holder and couple therewith. However, Bruner clearly fails to teach forming at least two channels through *a semiconductor device package* from a first major surface thereof to a second, opposing major surface thereof, or *aligning the at least two channels formed in the semiconductor device package with the at least two alignment features of the carrier substrate.* As such, Applicant submits that claim 1 is clearly not anticipated by Bruner.

Applicant further submits that claims 12 through 16 are allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 12 through 14, Applicant submits that Bruner fails to teach placing a semiconductor device package over a carrier substrate using a pick and place device.

With respect to claims 13 and 14, Applicant submits that Bruner fails to teach inserting pins carried by the head of the pick and place device through the at least two channels and the at least two holes.

With respect to claim 14, Applicant submits that Bruner fails to teach lifting the pick and place device, including the pins, from the aligned semiconductor device package and carrier substrate.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 1 and 12 through 16.

Claims 24 and 35 through 39

Independent claim 24, as amended herein, is directed to a method of testing a semiconductor device package having a plurality of discrete conductive elements disposed in a pattern on a surface thereof. The method comprises: providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements; *forming at least two channels in the semiconductor device package, each channel passing from a first surface thereof to a second, opposing surface thereof*; providing

the carrier substrate with at least two alignment features, each alignment feature respectively spaced and positioned in correspondence to one of the at least two channels; placing the semiconductor device package over the carrier substrate; a*ligning each channel of the at least two channels formed in the semiconductor device package with a corresponding alignment feature of the at least two alignment features of the carrier substrate*; electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality; and passing at least one electrical signal between the semiconductor device package and the carrier substrate. Applicant respectfully submits that Bruner fails to teach all of the limitations of claim 24 of the presently claimed invention.

Again, the Examiner cites Bruner as teaching "a method of aligning comprising: forming at least two channels (28) through a semiconductor device (2); providing a major surface of a carrier substrate (3) with at least two alignment features (12); placing the semiconductor device over the carrier substrate and aligning the at least two channel[s] with the at least two alignment features (see Figs. 1 and 5)." (Office Action, page 3). Applicant respectfully disagrees.

As set forth above, Bruner discloses a device for assembling and testing microelectronic circuit members. The device includes a lead frame holder (2), which the Examiner identifies as a semiconductor device, and a cap (3), which the Examiner identifies as a carrier substrate. A lead frame and substrate are disposed in the lead frame holder and the cap is coupled with the lead frame holder to apply relative pressure between the lead frame and substrate member. Latching members associated with the cap are configured to be disposed within holes of the lead frame member to effect such coupling.

However, Bruner clearly fails to teach forming at least two channels through *a semiconductor device* package from a first major surface thereof to a second, opposing major surface thereof, or *aligning the at least two channels formed in the semiconductor device package with the at least two alignment features of the carrier substrate*. As such, Applicant submits that claim 24 is clearly not anticipated by Bruner.

Applicant further submits that claims 35 through 39 are allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 35 through 37, Applicant submits that Bruner fails to teach placing a semiconductor device package over a carrier substrate using a pick and place device.

With respect to claims 36 and 37, Applicant submits that Bruner fails to teach inserting pins carried by the head of the pick and place device through the at least two channels and the at least two holes.

With respect to claim 37, Applicant submits that Bruner fails to teach lifting the pick and place device, including the pins, from the aligned semiconductor device package and carrier substrate.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 24 and 35 through 39.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,228,862 to Baumberger et al. in View of U.S. Patent No. 3,678,385 to Bruner

Claims 10, 11, 33, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baumberger et al. (U.S. Patent No. 5,228,862) in view of Bruner (U.S. Patent No. 3,678,385). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of are improper because the references relied upon by the Examiner fail to teach or suggest all of the limitations of the presently claimed invention.

Claims 10 and 11

Each of claims 10 and 11 depend from independent claim 1 by way of intervening claims. Applicant submits that Baumberger and Bruner fail to teach or suggest all of the limitations of independent claim 1. As set forth above, both Baumberger and Bruner fail to teach or suggest forming at least two channels through *the semiconductor device* package from a first major surface thereof to a second, opposing major surface thereof, or aligning the at least two channels *formed in the semiconductor device package* with the at least two alignment features of the carrier substrate.

As such, Applicant submits that claims 10 and 11 are allowable over Baumberger and Bruner at least by virtue of their dependency from an allowable base claim and respectfully requests reconsideration thereof.

Claims 33 and 34

Each of claims 33 and 34 depend from independent claim 24 by way of intervening claims. Applicant submits that Baumberger and Bruner fail to teach or suggest all of the limitations of independent claim 24. As set forth above, both Baumberger and Bruner fail to teach or suggest forming at least two channels through *the semiconductor device* package from a first major surface thereof to a second, opposing major surface thereof, or aligning the at least two channels *formed in the semiconductor device package* with the at least two alignment features of the carrier substrate.

As such, Applicant submits that claims 33 and 34 are allowable over Baumberger and Bruner at least by virtue of their dependency from an allowable base claim and respectfully requests reconsideration thereof.

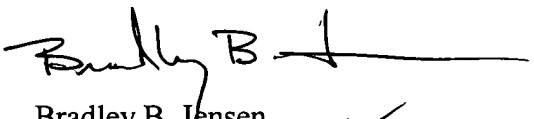
ENTRY OF AMENDMENTS

The amendments to claims 1, 6, 8, 9, 12-14, 18, 22-24, 29, 31, 32, 35, 37, 41, 45 and 46 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1, 3 through 8, 10 through 16, 24, 26 through 31, and 33 through 39 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Bradley B. Jensen
Registration No. 46,801
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: August 29, 2003
BBJ/ps:djp
Document in ProLaw